Evaluation of Switching Behavior of SiC JFET Based on Static I-V and C-V Characteristics

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Abstract

Transient response of junction field-effect transistors (JFETs) at switching operation is governed by static *I-V* characteristics and parasitic capacitances. This paper aims to model the switching behavior of lateral-type and vertical-type silicon carbide (SiC) JFETs based on their static *I-V* characteristics and capacitances between terminals. To this end, this paper characterizes and models these characteristics for both types of SiC JFET. Finally, the simulation results are compared with experimental results.

Keywords: SiC JFET, device model, transient response, static *I-V* characteristics, *C-V* characteristics

1. Introduction

Recently, SiC-based semiconductor devices are strongly required to be alternative to silicon (Si) devices for its superior material characteristics in stable operation at high temperature, high switching speed, and high withstand voltage [1][2]. And also, lateral-type and vertical-type SiC JFETs [2]-[5] have been developed. Figure 1(b) shows the cross section of the lateral-type SiC JFET, which is different from the conventional JFET [6][7]. There is a buried p^+ gate section at the top and p^- substrate section at the bottom, whose separation determines the n-channel thickness. The top p^+ and bottom p^- layers create pn junctions with n-type channel. Figure 1(c) shows the cross section of the vertical-type SiC JFET. There is a buried p^+ gate section at the top of the drift region that is connected to the source terminal. It constitutes a pn junction between the source and the n^- drift region. The equivalent capacitances between terminals are shown in Fig. 1(a). The characteristics of the switching device must be analyzed and modeled before JFET-based applications can be designed and built.

The switching behavior of the lateral-type and vertical-type SiC JFET is discussed with their internal capacitances, drain-source current I_{DS}, total current I_T, gate current I_G, gate-source voltage V_{GS}, and drain-source voltage V_{DS}, which are shown in Fig. 1(a). The gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} must be charged and discharged by the gate drive circuit for switching operation. The drain-source capacitance C_{DS} also affects on the switching speed.

A model of semiconductor device is indispensable for evaluating the voltage and current response at switching in circuit simulation and estimating the system performance in their applications. Those are the targets of our research for modeling, which has not been achieved yet. The dynamics at the transient state are obviously governed by these characteristics of devices.

Therefore, this paper characterizes and models the static *I-V* and *C-V* characteristics of SiC JFET, and compares these characteristics between the lateral-type and vertical-type SiC JFET based on physical structure of the devices. Next, this paper discusses the *C-V* and switching characteristics based on their device structure and the semiconductor physics. In the end, the simulated switching behaviors of both SiC JFETs are validated with the experimental results.

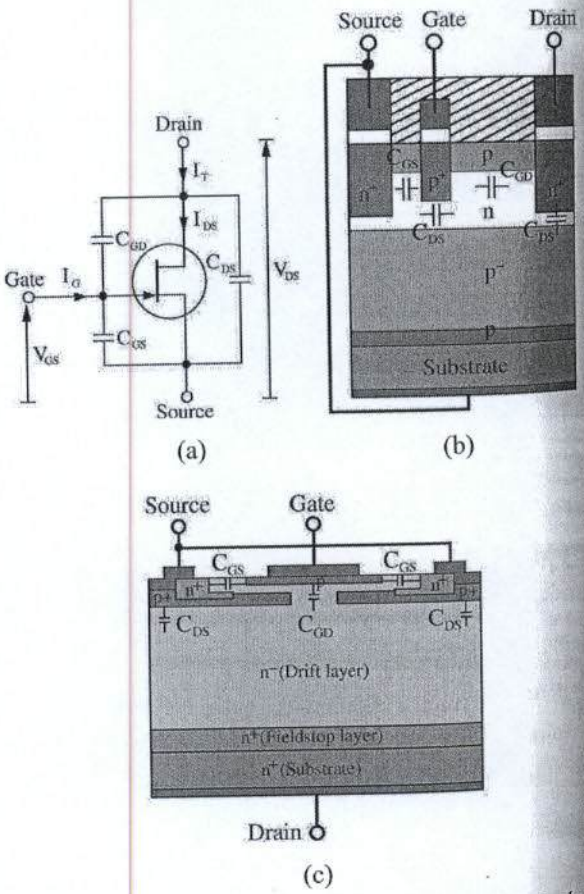


Fig. 1 (a) Equivalent capacitances between terminals of JFET, (b) cross section of lateral-type SiC JFET cell, and (c) cross section of vertical-type SiC JFET cell.

2 SiC JFET Model

2.1 Static *I-V* Characteristics of SiC JFET

Figures 2(a) and (b) show the measured static *I-V* characteristics of lateral-type SiC JFET and vertical-type SiC JFET, respectively, for different values of gate-source voltage V_{GS} at room temperature (25°C). The both of SiC JFETs studied in this paper are normally-on. The steady-state forward *I-V* characteristics of both SiC JFETs are drawn by pentode like curves to the gate-source voltage V_{GS}. The relationship between the drain-source current I_{DS} and the drain-source voltage V_{DS} is modeled at the steady-state as a function of V_{GS} and V_{DS} as Eq. (1) [5]-[7]:

$$I_{DS} \cong \begin{cases} \dfrac{\beta((V_{GS}-V_T)V_{DS}-V_{DS}^2/2)}{(1+\theta(V_{GS}-V_T))} & \text{for } V_{DS} \le V_{GS}-V_T \\ \dfrac{\beta(V_{GS}-V_T)^2}{2(1+\theta(V_{GS}-V_T))} & \text{for } V_{DS} > V_{GS}-V_T \end{cases} \quad (1)$$

Here, β denotes the JFET channel transconductance, V_T the threshold voltage, and θ the mobility modulation coefficient. In this model, the effect of drain resistance R_D and source resistance R_S is neglected.

2.2 *C-V* Characteristics of SiC JFET

Figures 1(b) and (c) showed the cross section of one cell in the lateral-type SiC JFET and vertical-type SiC JFET, respectively. The depletion layer and the undepleted region of the semiconductor, which are connected to electrodes, constitute the capacitance of the devices between terminals. They are lumped into three combinations of capacitances between terminals, which are the gate-source C_{GS}, the gate-drain C_{GD}, and the drain-source capacitances C_{DS}, as depicted in Fig. 1(a). The thickness of depletion layer changes with the applied voltage between terminals (V_{GS} and V_{DS}), and results in the change of differential capacitances in the switching operation. Therefore, the *C-V* characteristics can be described by depletion layer capacitances as in Eqs. (2)-(4) [6][7][9]:

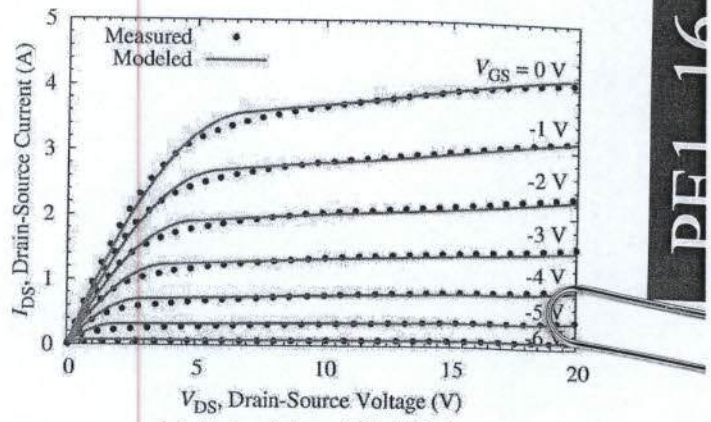
$$C_{GS} = C_{GS}(0), \quad (2)$$

$$C_{GD} = C_{GD}(0)\left(1+\frac{V_{DS}}{\phi_{0_{GD}}}\right)^{-m_{GD}}, \quad (3)$$

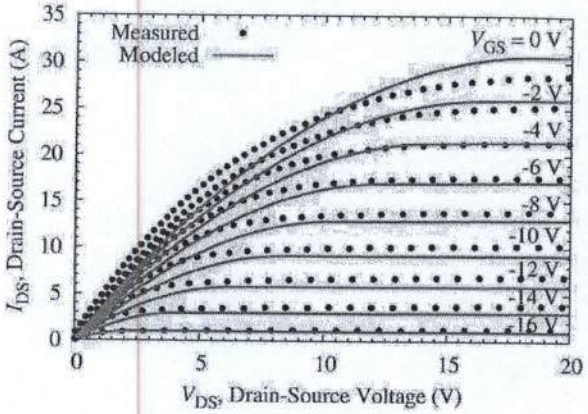
$$C_{DS} = C_{DS}(0)\left(1+\frac{V_{DS}}{\phi_{0_{DS}}}\right)^{-m_{DS}}, \quad (4)$$

where $C_{GS}(0)$, $C_{GD}(0)$, and $C_{DS}(0)$ denote the zero-bias capacitance of gate-source, gate-drain, and drain-source, respectively. $\phi_{0_{GD}}$ denotes the gate-drain junction potential, $\phi_{0_{DS}}$ the drain-source junction potential, m_{GD} the junction grading coefficient of impurity concentration, and m_{DS} the junction grading coefficient of impurity concentration.

Both SiC JFETs are limited to the normally-on type as mentioned above. The lateral-type SiC JFET has 200 V blocking voltage and the rated 5 A drain current. The vertical-type SiC JFET has 900 V blocking voltage and the rated 2.5 A drain current.

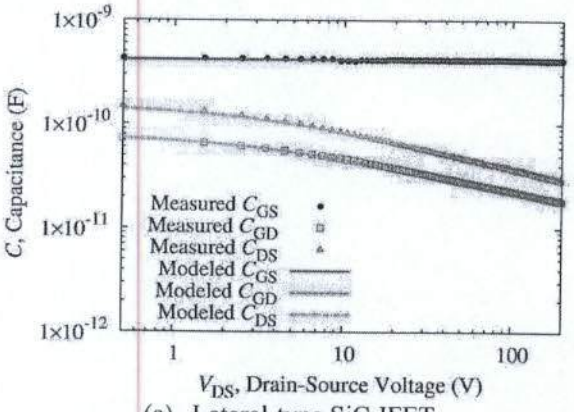


(a) Lateral-type SiC JFET

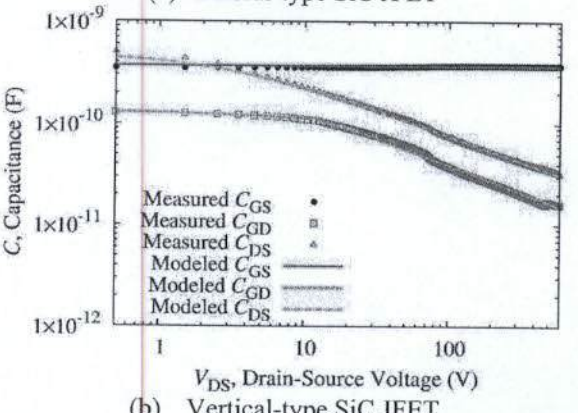


(b) Vertical-type SiC JFET

Fig. 2 Static *I-V* characteristics of SiC JFET



(a) Lateral-type SiC JFET



(b) Vertical-type SiC JFET

Fig. 3 *C-V* characteristics of SiC JFET

In the experimental setup for characterization, the *C-V* characteristics of both devices are precisely measured by a *LCR* meter with applying dc bias voltages V_{GS} and V_{DS} to the devices, through *C-V* measurement fixture in Ref. [8]. The measurements are performed with applying V_{DS} = 0 V to avoid short circuit current for V_{GS} dependency, and V_{GS} = −20 V to block the channel of devices for V_{DS} dependency. For the measurement of V_{DS} dependency, V_{DS} is swept from 0 V to 200 V for lateral-type and from 0 V to 600 V for vertical-type.

The measured and modeled C-V_{DS} characteristics for both SiC JFETs are shown in Figs. 3(a) and (b). C_{GS} hardly changes with the variation of VDS. The values are around 415 pF for lateral-type and 368 pF for vertical-type. Because the electric fields induced by V_{DS} does not affect on the electric field across gate and source due to the fixed V_{GS}. On the other hand, C_{GD} and C_{DS} decrease smoothly according to the increase of V_{DS}. The extracted capacitance model parameters of C_{GD} and C_{DS} are $C_{GD}(0)$ = 77 pF, m_{GD} = 0.34 and $C_{DS}(0)$ = 148 pF, m_{DS} = 0.38 for lateral-type, respectively. They are $C_{GD}(0)$ = 278 pF, m_{GD} = 0.55 and $C_{DS}(0)$ = 481 pF, m_{DS} = 0.52 for vertical-type, respectively. For the lateral-type in Fig. 1(b), C_{GD} and C_{DS} change slightly with the variation of V_{DS}, because the depletion region expands from the linearly graded doped n-region to p^+ gate and n-region to p-region, respectively. For the vertical-type in Fig. 1(c), the n-channel is aligned in horizontal-axis, but the n-type semiconductor (n^- drift region) is aligned in vertical axis. Therefore, C_{GD} has almost constant around 132 pF at V_{DS} ≤ 13 V, because the depletion region expands around channel opened between buried p^+ regions for low V_{DS}. Then, C_{GD} changes substantially with the variation of V_{DS} when V_{DS} > 13 V, because the depletion region expands from the p gate to the uniformly doped drift region. C_{DS} also changes substantially with the variation of V_{DS} in the low and high voltage ranges. It is because the depletion region expands from under the buried p^+ region to the uniformly doped drift region.

2.3 Switching Behavior of SiC JFET

The differential capacitances between terminals of the SiC JFET shown in Fig. 1(a) depend mainly on the applied terminal voltage in semiconductor shown in Figs. 1(b) and (c). The switching behavior of the SiC JFET is governed by these capacitances which are expressed as the functions of the relative voltages between each of the terminals. Eventually, the dynamical equations both SiC JFETs can be given by Eqs. (5) and (6) at charging/discharging states of the capacitances [7][9].

$$\frac{dV_{GS}}{dt} = \frac{I_G}{C_{GS}+C_{GD}} + \frac{C_{GD}}{C_{GS}+C_{GD}} \cdot \frac{dV_{DS}}{dt}, \quad (5)$$

$$\frac{dV_{DS}}{dt} = \frac{I_T - I_{DS} + \frac{C_{GD}}{C_{GS}+C_{GD}} I_G}{C_{DS}+C_{GD} - \frac{C_{GD}^2}{C_{GS}+C_{GD}}}. \quad (6)$$

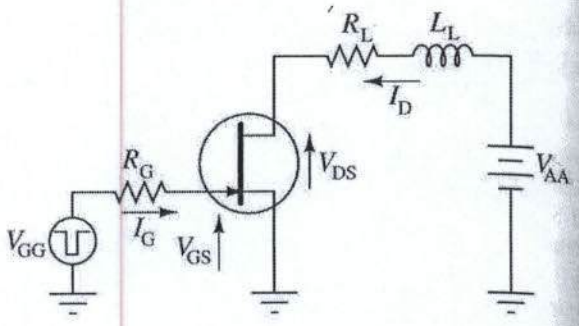
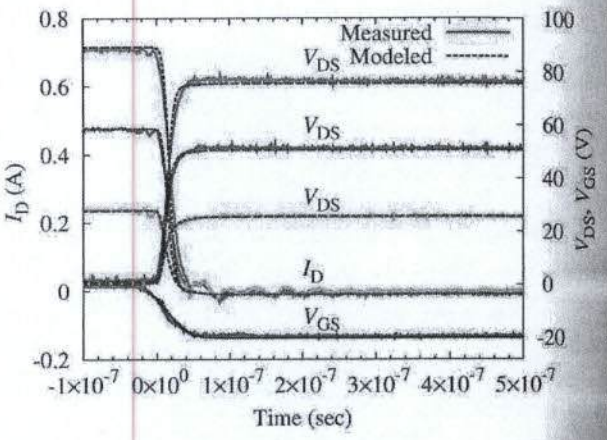
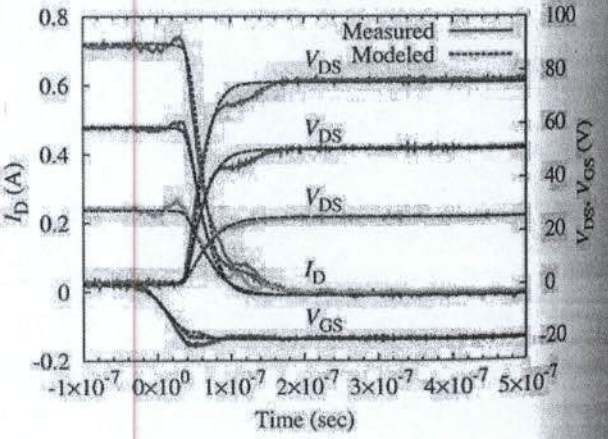


Fig. 4 Inductive load circuit for measured switching behavior



(a) Lateral-type SiC JFET



(b) Vertical-type SiC JFET

Fig. 5 Switching behavior of SiC JFET

3 Evaluation of Switching Behavior

The switching behavior of both devices is evaluated with the inductive load circuit, which is shown in Fig. 4. Then V_{DS}, V_{GS}, and I_D are measured in the experiments. V_{AA} is varied with setting three different V_{DS} at 25 V, 50 V, and 75 V. Here, L_L is set at 200 nH and R_L at 103 Ω. V_{GG} applied to the gate of JFET through R_G 5 Ω is switched between 0 V and −20 V. This paper especially discusses the derivative of the VDS, dV_{DS}/dt, in Eq. (6) depends on C_{GD}+C_{DS} with variation of V_{DS}. It affects on the switching behaviors when $V_{GS} < V_T$ (cut-off condition). The derivatives of the

V_{DS}, dV_{DS}/dt for lateral-type in Fig. 5(a) at V_{DS} = 25 V, 50 V, and 75 V correspond to 7.89×10^8 V/s, 20.42×10^8 V/s, and 33.67×10^8 V/s by the model. They are 8.00×10^8 V/s, 17.06×10^8 V/s, and 23.88×10^8 V/s in the measurement. The derivatives of the V_{DS}, dV_{DS}/dt , for vertical-type in Fig. 5(b) at V_{DS} = 25 V, 50 V, and 75 V correspond to 3.07×10^8 V/s, 8.05×10^8 V/s, and 14.03×10^8 V/s by the model. They are 2.60×10^8 V/s, 5.71×10^8 V/s, and 10.47×10^8 V/s in the measurement. The model accurately explains the experimental results. The accumulated charges Q, calculated from drain voltage dependency of capacitance at V_{DS} = 25 V, 50 V, and 75 V, are equal to 3.27 nC, 5.35 nC, and 7.09 nC for lateral-type in Fig. 3(a). Those are 8.42 nC, 13.33 nC, and 17.12 nC for vertical-type in Fig. 3(b). The ratios of the derivative of the V_{DS}, dV_{DS}/dt, between lateral-type and vertical-type are equal to 2.57, 2.53, and 2.40. The ratios of Q between both types are equal to 1/2.57, 1/2.50, and 1/2.41. Therefore, the ratio of turn-off speed of V_{DS} between SiC JFETs depends on the inverse ratio of Q. The lateral-type shows about 2.5 times faster turn-off speed than the vertical-type. Because the lateral-type has smaller C_{DS} and C_{GD} than the vertical-type as mentioned above.

4 Conclusions

This paper characterized and discussed the switching behavior of SiC JFETs based on the static *I-V* and *C-V* characteristics. The difference between the switching characteristics of the lateral-type and the vertical-type SiC JFETs depends on their internal parasitic capacitances, which can be classified by the dependence of depletion capacitance. Therefore, the device structure and switching phenomenon can be characterized and explained for these SiC JFETs by the measurement of *C-V* characteristics of devices. The simulated results of the switching behavior well agree with the experimental results for some conditions of the model and extracted parameter from the *C-V* and *I-V* characteristics of these devices.

6. Acknowledgment

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